In the United States Patent and Trademark Office

In re the application of
Lee D. Whetsel — TI-27442.2

Application No. 10/816,073 — Art Unit: 2138
Confirmation No. 8884

Filed: 3/31/2004 — Examiner: David Ton

Title: Position Independent Testing of Circuits

Amendment B Under 37 CFR 1.111

April 19, 2006

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

Responsive to the Examiner's Action of 10/19/2005, please amend this application as follows:

In the Title:

Amend the title as follows:

~~Position Independent Testing of Circuits~~ IC With Scan Distributor and Scan Collector Circuitry

In the Claims:

1. (original) An integrated circuit comprising:

A. core circuitry including functional inputs and functional outputs;

B. an input pad;

C. scan distributor circuitry connected between the input pad and, selectively, at least some of the functional inputs;

D. an output pad; and

E. scan collector circuitry connected selectively between at least some of the functional outputs and the output pad.

2. (original) The integrated circuit of claim 1 including controller circuitry connected to the scan distributor circuitry, the scan collector circuitry and the core circuitry.

3. (original) The integrated circuit of claim 1 including multiplexer circuitry selectively connecting the scan distributor circuitry to at least some of the functional inputs.

4. (original) The integrated circuit of claim 1 including demultiplexer circuitry selectively connecting at least some of the functional outputs to the scan collector circuits.

5. (original) The integrated circuit of claim 1 including plural core circuits, each with its own scan distributor and collector circuits selectively connected to at least some of the respective functional inputs and outputs.

6. (original) The integrated circuit of claim 1 including plural core circuits, each with its own scan distributor and collector circuits selectively connected to at least some of

the respective functional inputs and outputs, the scan distributor and collector circuits of one core circuitry being connected in a hierarchy with the scan distributor and collector circuits of another core circuit.

7. (original) Integrated circuit core circuitry comprising:

A. functional circuitry having plural functional inputs and plural functional outputs and including parallel scan paths;

B. scan distributor circuitry having a serial input connected to a functional input and a serial output connected to a functional output and having parallel outputs connected to inputs of the parallel scan paths; and

C. scan collector circuitry having a serial input connected to a functional input and a serial output connected to a functional output and parallel inputs connected to outputs of the parallel scan paths.

8. (original) An integrated circuit including plural core circuitry of claim 7 including functional outputs of one core circuitry being connected to functional inputs of another core circuitry and functional outputs of the another core circuitry connected to the functional inputs of the one core circuitry to connect the serial output of one scan distributor to the serial input of another scan distributor and to connect the serial output of one scan collector to the input of another scan collector.

9. (original) The integrated circuit of claim 8 including multiplexer and demultiplexer circuitry selectively connecting the functional outputs to the functional inputs.

10. (original) The integrated circuit of claim 8 in which the serial output of the one scan distributor connects through one functional output and functional inputs of plural cores to the serial input of plural scan distributors.

11. (original) The integrated circuit of claim 8 in which the serial output of plural scan distributors connects

through plural functional outputs and one functional input to the serial input of the one scan distributor.

12. (original) The integrated circuit of claim 8 in which the serial input of the one scan collector connects through one functional input of the one core and plural functional outputs of plural cores to the serial output of plural scan collectors.

13. (original) The integrated circuit of claim 8 in which the serial output of the one scan collector connects through one functional output and plural functional inputs to the serial input of plural scan collectors.

14-23. (cancelled)

Remarks

Applicant thanks the Examiner for the careful examination of this application and the clear explanation of the rejections.

The amended title is clearly indicative of the invention to which the claims are directed.

Applicant submits PTO/SB/26 (09-04), Terminal Disclaimer to Obviate a double patenting Rejection over a "Prior" Patent, US 6,405,335. This terminal disclaimer overcomes the obviousness-type double patenting rejection and places the application in condition for allowance.

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests reconsideration or further examination of this application.

Respectfully Submitted,

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